New Booster Corrector Magnet

Power Amplifier Controls

Draft Specification

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General Specification

We are planning to install 48 new corrector magnet packages into the Booster in the Fall of 2007. Each of these packages contains 6 magnets, for a total of 288 magnets and associated power amplifiers. The power amplifiers and associated control electronics will be distributed into 6 locations around the Booster Gallery. The power amplifier controls in each of the 6 locations will need to support the functions for 48 power amplifiers. We are requesting new electronics to provide the following functionality for each power amplifier.

1. Provide an ACNET programmable DAC ramp voltage output with the following parameters.
    a. +/- 10V output into >20K Ohms.
    b. 10 k updates per second.
    c. At least 400 points per curve.
    d. At least 10 different curves for use with different Booster modes.
    e. 16 Bit nominal DAC resolution.

2. Provide analog readback for four voltages per power amplifier.
    a. +/- 10V input.
    b. 10 k updates per second.
    c. 16 Bit nominal ADC resolution.

3. Provide a function to compare the desired current setting determined by the DAC ramp values with the current monitor read back to determine if the power amplifier is sufficiently tracking the desired ramp. A status back to ACNET will indicate whether the power amplifier is tracking.

4. Besides the programmable table of ramp values, a separate DC current bias value will be settable in ACNET that will be summed with the ramp values.

5. Provide four digital outputs capable of driving a TTL level at >40mA for use as the power amplifier ACNET Enable/Inhibit.

6. Four digital logic interlock inputs should be available on the module to be summed with the results of the amplifier tracking comparison (Item 3.) that will inhibit the output of power amplifier. These inputs will be derived from temperature threshold comparisons, power amplifier failure indications, door interlocks, flow switches, etc.

7. Provide for read back to ACNET of eight status bits (TTL at < 10 mA source current) for each power amplifier.

8. Provide the ability in ACNET to load ramp curves from an ASCII text file.

9. For the sake of 15 Hz Booster operation, processing time available between the playing of the ramps is 20 ms.

Current Design Proposal

It is proposed that a new CAMAC module be design to perform the functionality listed in the General Specification, except the measurement of the four analog voltages per power amplifier. The analog voltage monitoring would be performed using the MADC functionality of the HRM rack monitor chassis. The CAMAC module would actually be a two module set; one board with a processor and the other with the analog and digital IO, the tracking comparison, and the interlock Inhibit chain. Appendix A contains a listing of the IO connections available on the rear of the module.

APPENDIX A

Preliminary Booster Corrector Controller I/O Proposal – A. Franck – 6/22/05

"A" Board Viking Connector

1L – MDAT Digital Gnd
1R – TCLK Digital Gnd
2L – TCLK Output
2R – TCLK Input
3L – MDAT Output
3R – MDAT Input

4L – TTL Output – Enable Supply 1
4R – TTL Output – Enable Supply 2
5L – Digital Gnd
5R – Digital Gnd
6L – TTL Output – Enable Supply 3
6R – TTL Output – Enable Supply 4

7L – Opto Anode Supply – 5 Volts provided by Supply 1
7R – Status Input 1-1 – (pull low for active state)
8L – Status Input 1-2
8R – Status Input 1-3
9L – Status Input 1-4
9R – Status Input 1-5
10L – Status Input 1-6
10R – Status Input 1-7
11L – Status Input 1-8
11R – Status Input 1-9
12L – Status Input 1-10
12R – Status Input 1-11

13L – Opto Anode Supply – 5 Volts provided by Supply 2
13R – Status Input 2-1 – (pull low for active state)
14L – Status Input 2-2
14R – Status Input 2-3
15L – Status Input 2-4
15R – Status Input 2-5
16L – Status Input 2-6
16R – Status Input 2-7
17L – Status Input 2-8
17R – Status Input 2-9
18L – Status Input 2-10

18R – Status Input 2-11

"B" Board Viking Connector

1L – Analog Reference Output 1
1R – Analog Reference Ground 1
2L – Analog Current Readback 1

2R – Analog Reference Output 2
3L – Analog Reference Ground 2
3R – Analog Current Readback 2

4L – Analog Reference Output 3
4R – Analog Reference Ground 3
5L – Analog Current Readback 3

5R – Analog Reference Output 4
6L – Analog Reference Ground 4
6R – Analog Current Readback 4

7L – Opto Anode Supply – 5 Volts provided by Supply 3
7R – Status Input 3-1 – (pull low for active state)
8L – Status Input 3-2
8R – Status Input 3-3
9L – Status Input 3-4
9R – Status Input 3-5
10L – Status Input 3-6
10R – Status Input 3-7
11L – Status Input 3-8
11R – Status Input 3-9
12L – Status Input 3-10
12R – Status Input 3-11

13L – Opto Anode Supply – 5 Volts provided by Supply 4
13R – Status Input 4-1 – (pull low for active state)
14L – Status Input 4-2
14R – Status Input 4-3
15L – Status Input 4-4
15R – Status Input 4-5
16L – Status Input 4-6
16R – Status Input 4-7
17L – Status Input 4-8
17R – Status Input 4-9
18L – Status Input 4-10
18R – Status Input 4-11